ACTIVE MEMORY PROCESSING ARRAY TOPOGRAPHY AND METHOD

ABSTRACT OF THE DISCLOSURE

An integrated active memory device includes an array of processing elements coupled to a dynamic random access memory device and to a component supplying instructions to the processing elements. The processing elements are logically arranged in a plurality of logical rows and logical columns. The array is logically folded to minimize the length of the longest path between processing elements by physically interleaving the processing elements so that the processing elements in different logical rows a physically interleaved with each other and the processing elements in different logical columns a physically interleaved with each other.